**ECE 385**

**Spring 2018**

Experiment #1

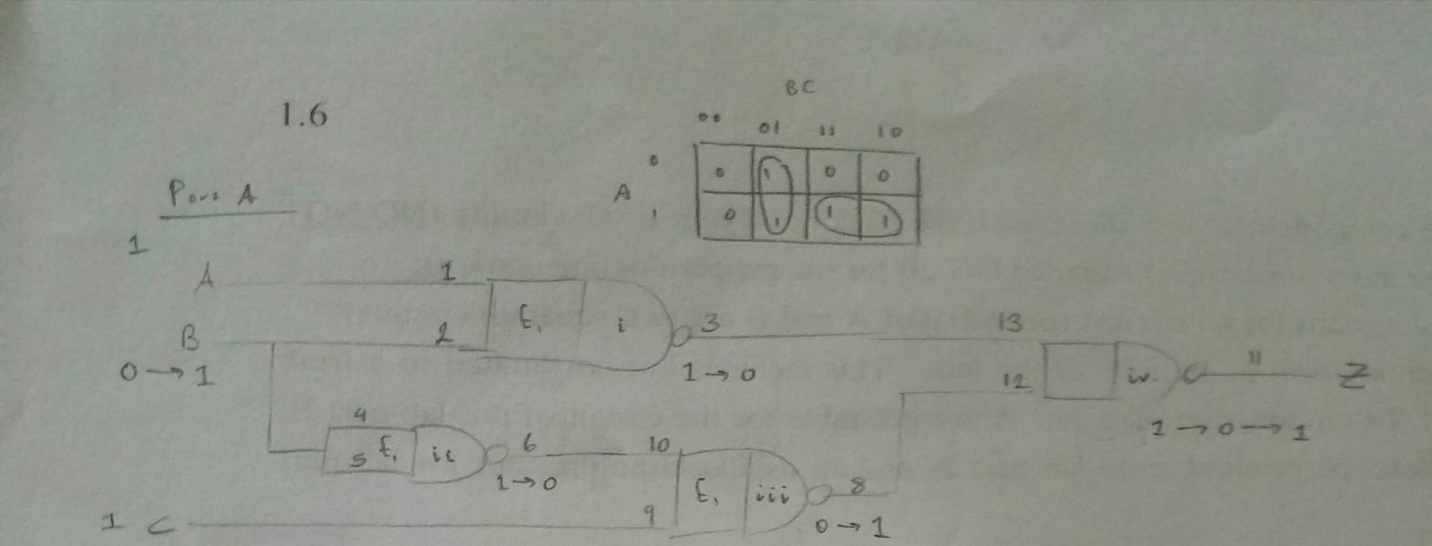
Sahil Shah

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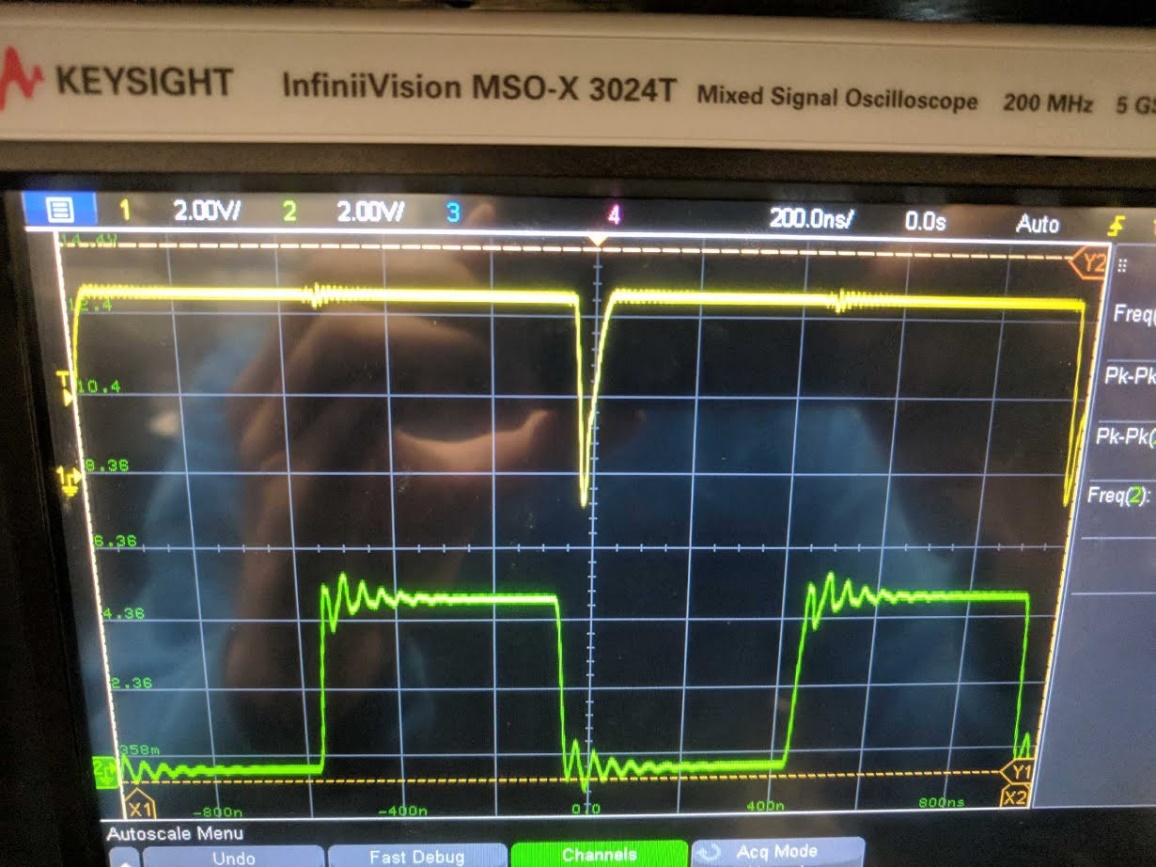
Introductory Experiment

Intro: The purpose of this lab is to discover and fix a ‘glitch’ in a 2-1 multiplexor. This lab is intended to familiarize us with the student lab kit, I/O boards, oscilloscope and pulse generator. This is achieved by observing propagation delay in TTL chips. The glitch observed in the 2-1 mux is found and fix in part A and B respectively in this lab.

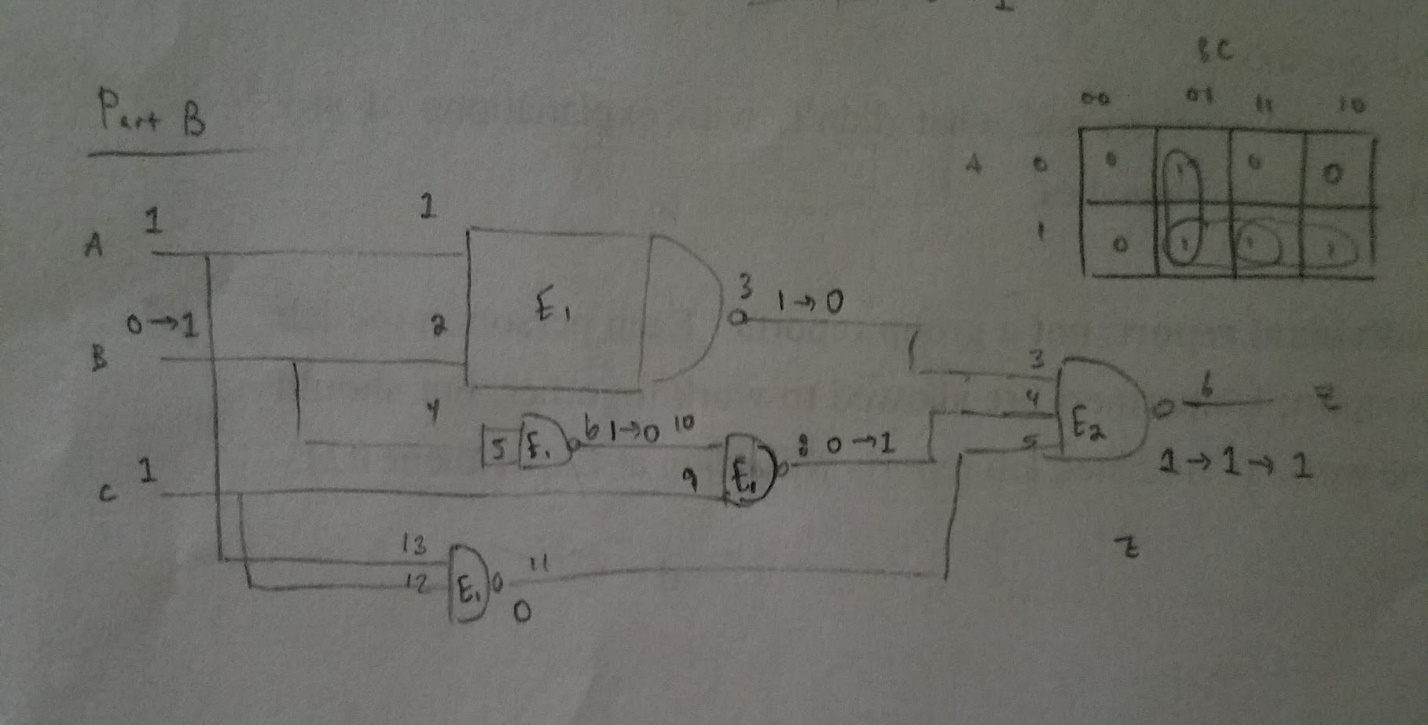
Circuit Description: A static one hazard occurs in the circuit in part A due to the propagation delay in the 2-level design.



This is shown by holding A and C high and driving B from 0 to 1. The output, Z starts high. After driving B from 0 to 1, the changes in the circuit are staggered due to the delay. After 20ns, NAND “i” and “ii” change to 0. Toggling B does not change Z immediately. After another 20ns, NAND “iii” changes to 1 and NAND “iv” changes to 0. This change in Z (the output of NAND “iv” is the glitch. Finally, after another 20ns, NAND “iv” changes back to 1. This glitch can be seen on the oscilloscope. On the rising edge of the input, a jump from 1 to 0 and back can be seen in the output.



A NAND gate only drops to 0 when both inputs are high. Therefore, by adding a third input that always stays high, the output, Z, will always stay high. Adding an extra gate with inputs A, C that connects to a 3-input NAND gate, as shown below, fixes the glitch seen in part A.



When taking propagation delay into account, the same conclusion can be reached. By setting A and C high and driving B from 0 to 1, the first gates to change are the 3 on the far left. This change occurs 20ns after B is driven high. After these gates change, the middle and far right gate changes. This occurs 40ns after B was driven high. The output, Z, after both changes is 1. Finally, the last change occurs due to the middle gate changing. This change occurs 60ns after B was driven high. The output, Z, remains 1. Driving B from 0 to 1 and keeping A and C high in this configuration does not produce a static one hazard, fixing the ‘glitch’ seen in the first part of this lab.



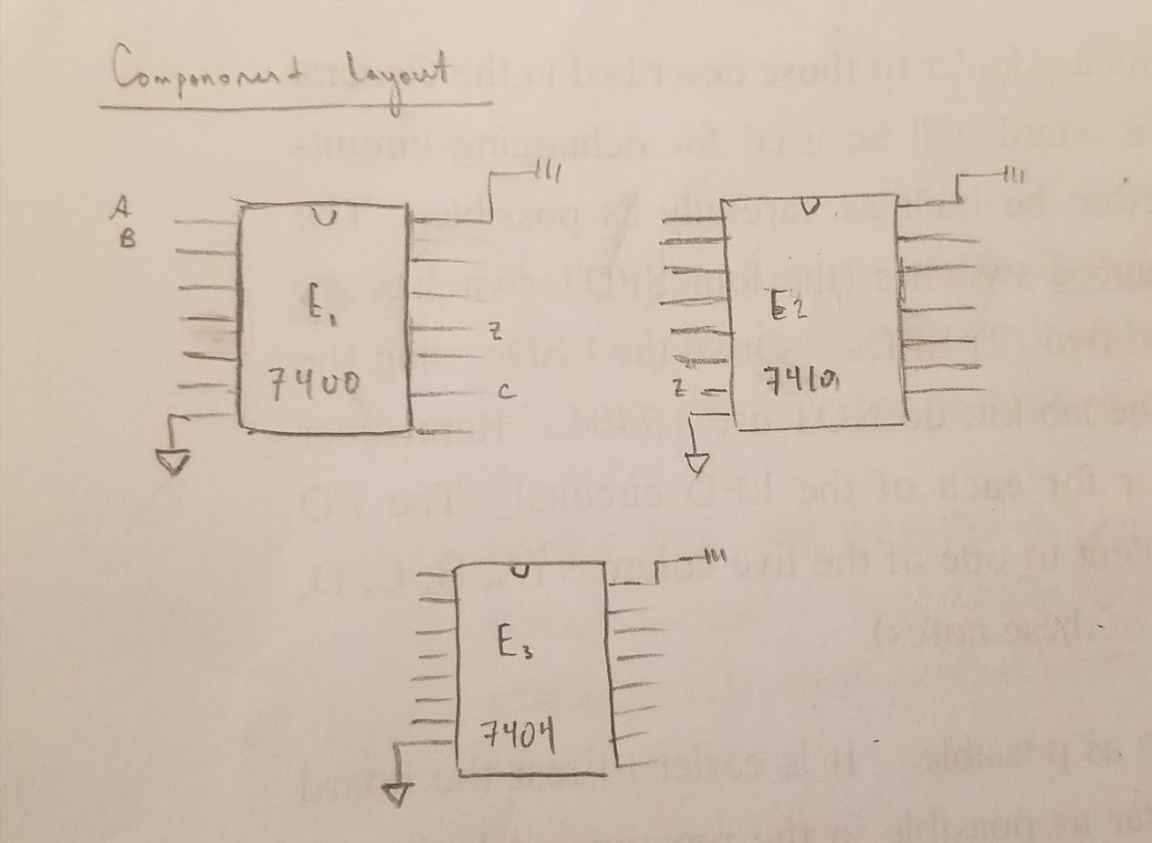
This is the truth table for parts A and B of this lab:

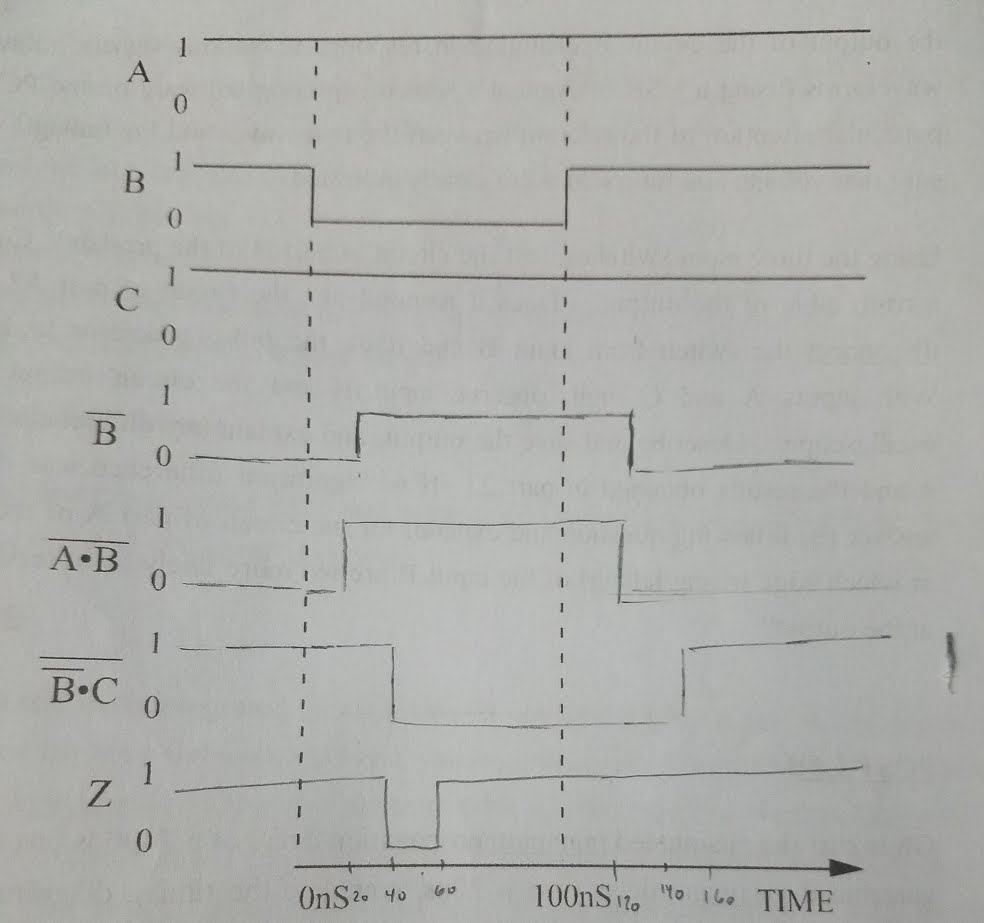


The output, Z, for both parts of the lab is the same.

Component Layout:

* E1: 7400 quadruple 2-input positive NAND gate
* E2: 7410 triple 3-input positive NAND gate
* E3: 7404 Hex inverter



Post-Lab Question:

1. Timing Diagram

As seen in the timing diagram, a glitch occurs in Z at 40ns. This glitch is in response to the falling edge of B and is known as a Static-1 hazard. This glitch stabilizes after 20ns, which is the propagation delay of these TTL chips. The delay in these chips causes the glitch seen in the timing diagram.

1. The need for a debounced switch stems from the contact bounce that comes when a switch is flipped. Without a debounced switch, contact bounce would give multiple cycles instead of the one intended by the user. To fix this, an S-R latch is used to hold the value at the output. By nature, the bounce is never enough to strike the other terminal, so the output of the latch remains the same.

Conclusion: Static one hazards occur due to a glitch in digital logic that stems from the propagation delay of gates in the circuit. To fix the glitch, an additional product term must be added into the logic. This can be seen by observing the Karnaugh Maps from parts A and B of this lab. Ideally, this circuit in part A should have seen the one glitch caused by chip delay. However, the oscilloscope reading shows more noise. This noise stems from imperfect chips and protoboards. This can be fixed by using better connections and equipment. In practice, this glitch occurs extremely fast. Therefore, it is necessary to extend the delay by adding an even number of hex inverters to view it. If a non-even number of inverters is added, the output is inverted, which is an undesired effect.